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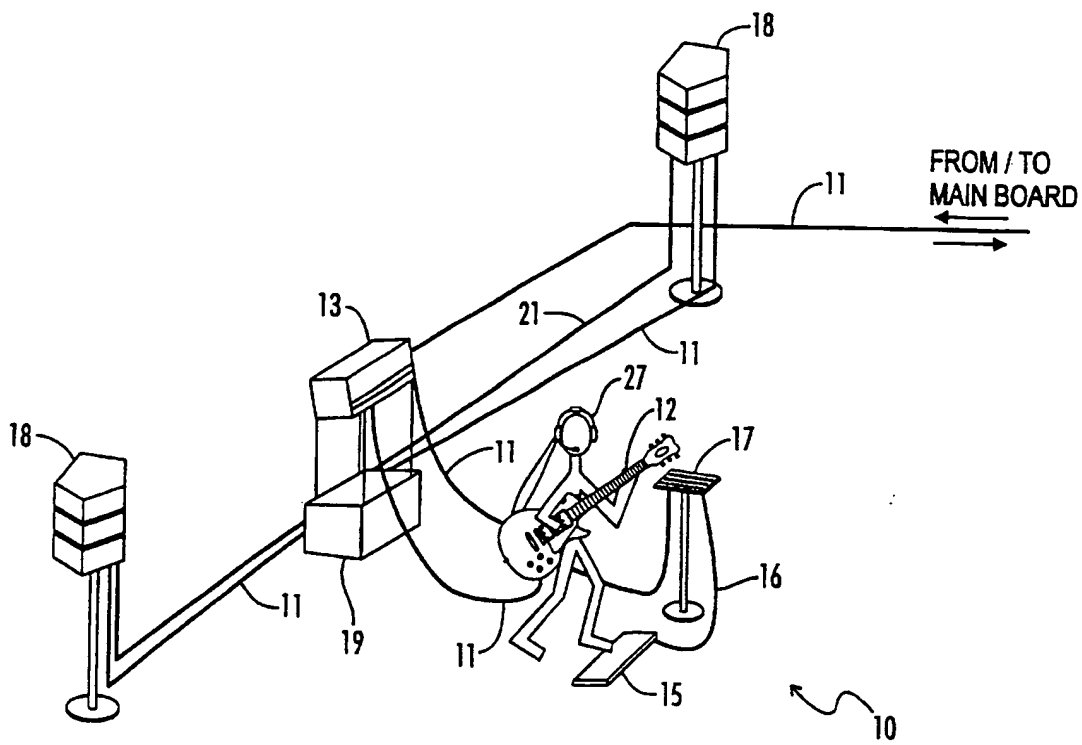
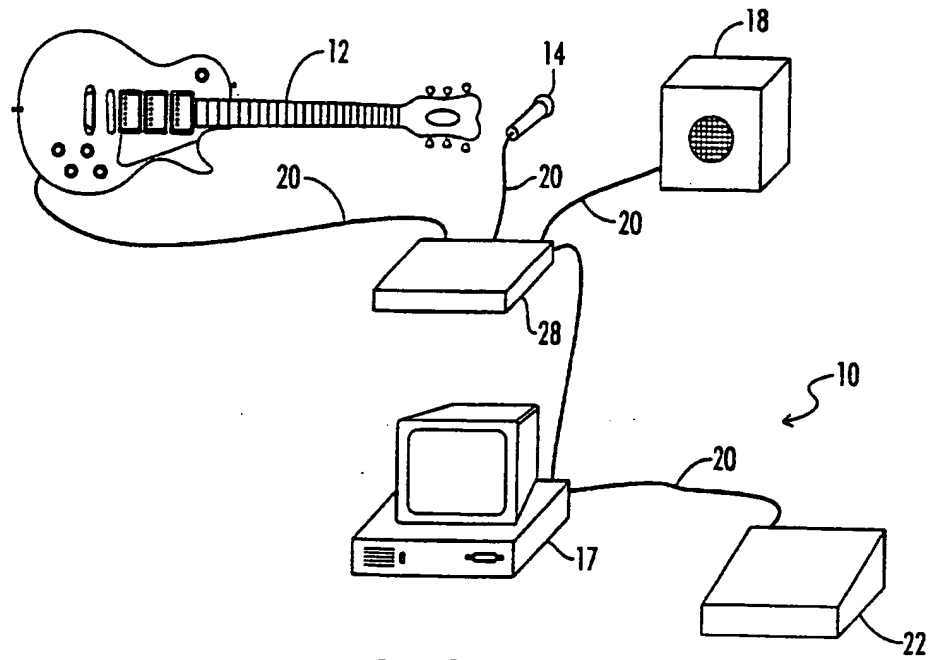
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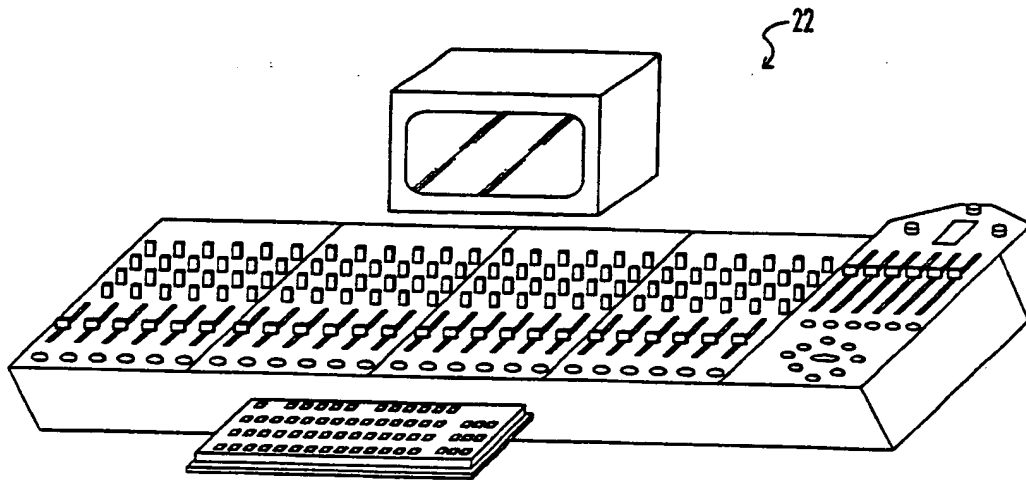


FIG. 3

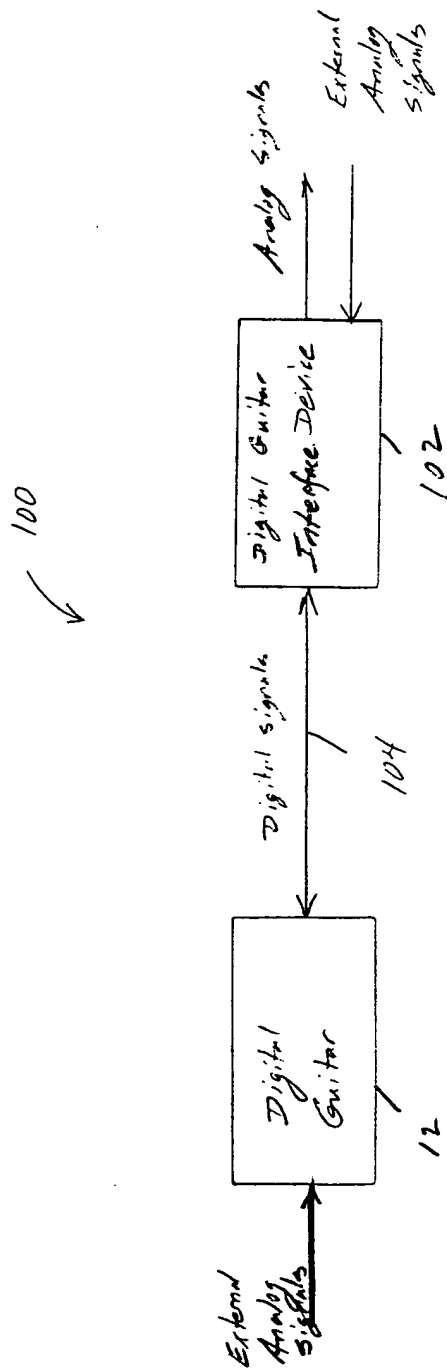


Fig. 4

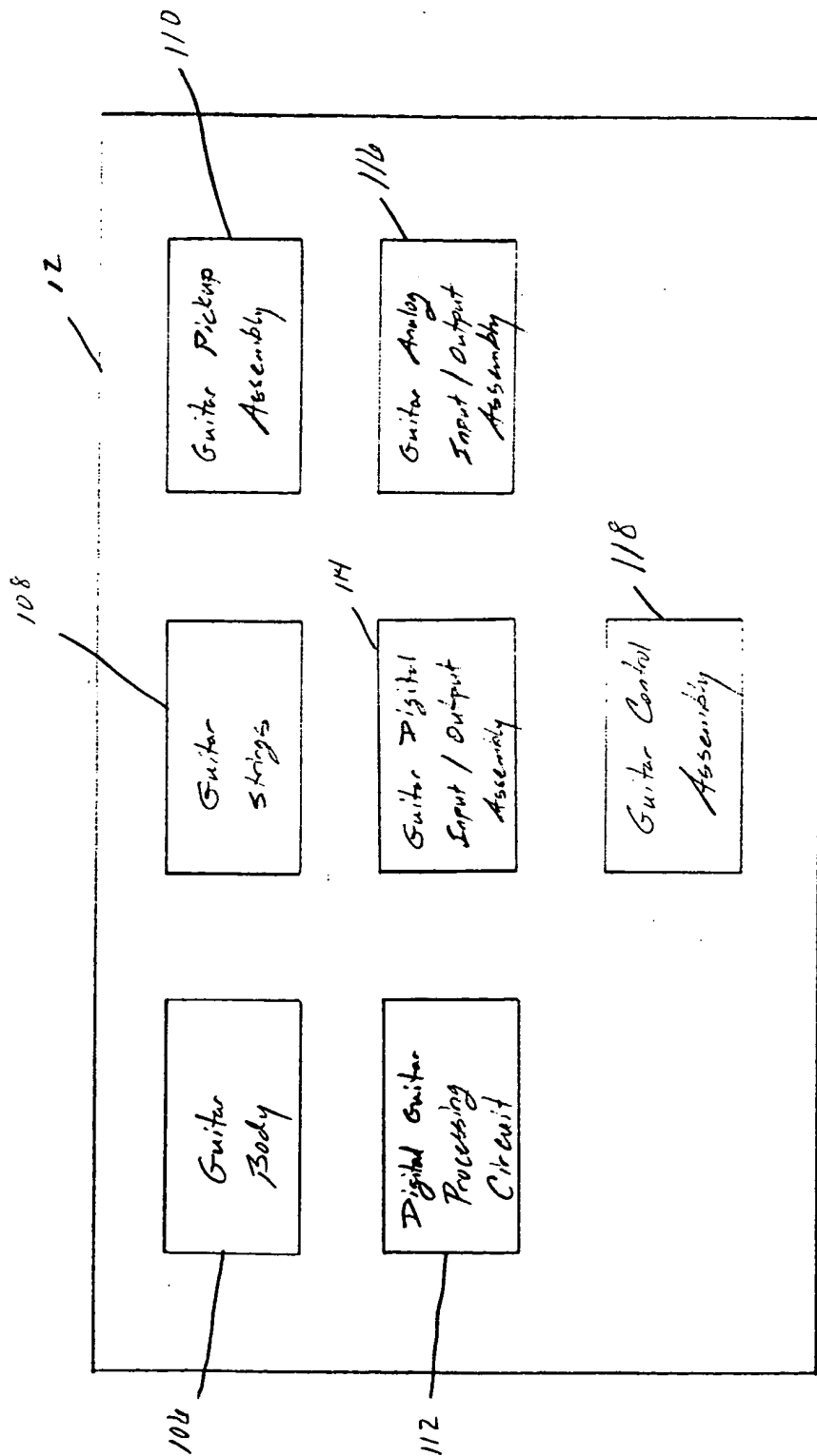


Fig. 5

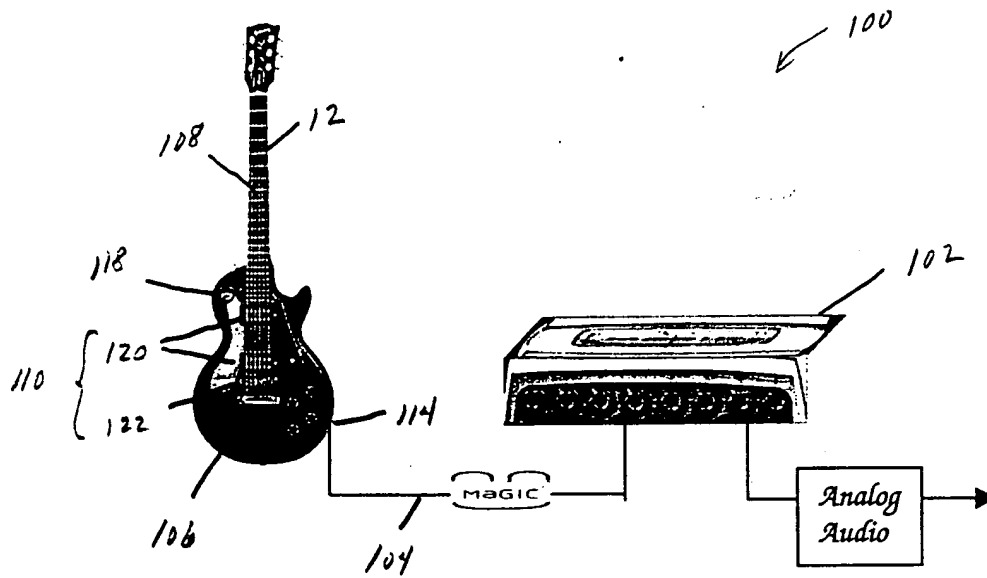


Figure 6

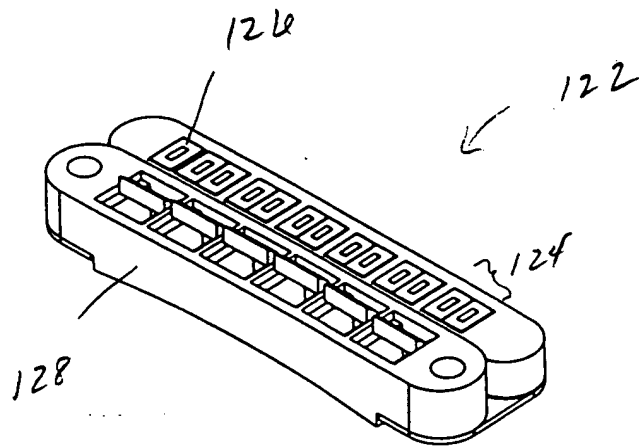


Fig. 7

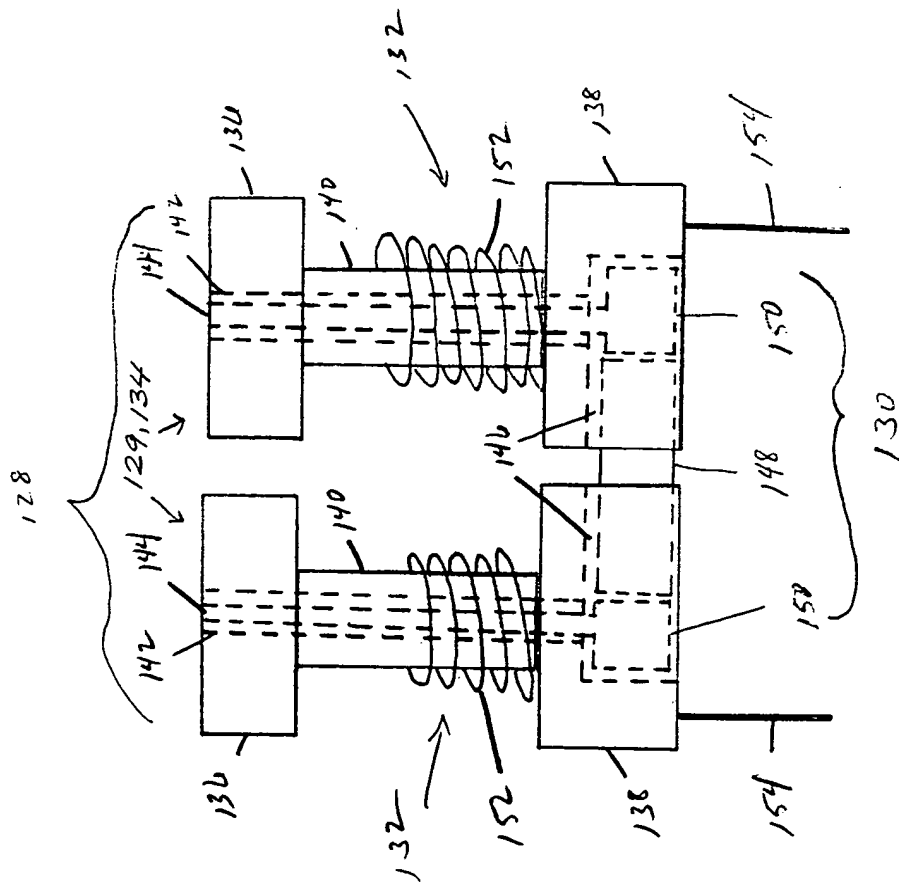


Fig. 8

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Digital Guitar Processing Circuit

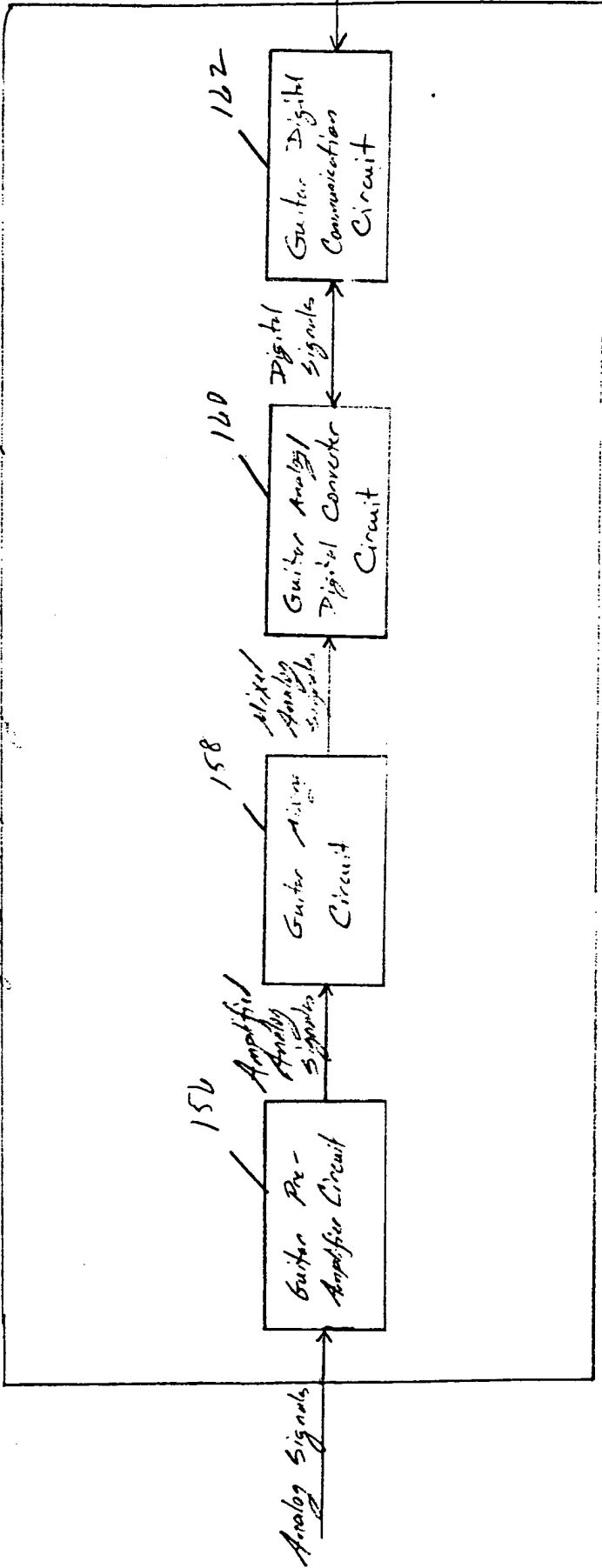


Fig. 9

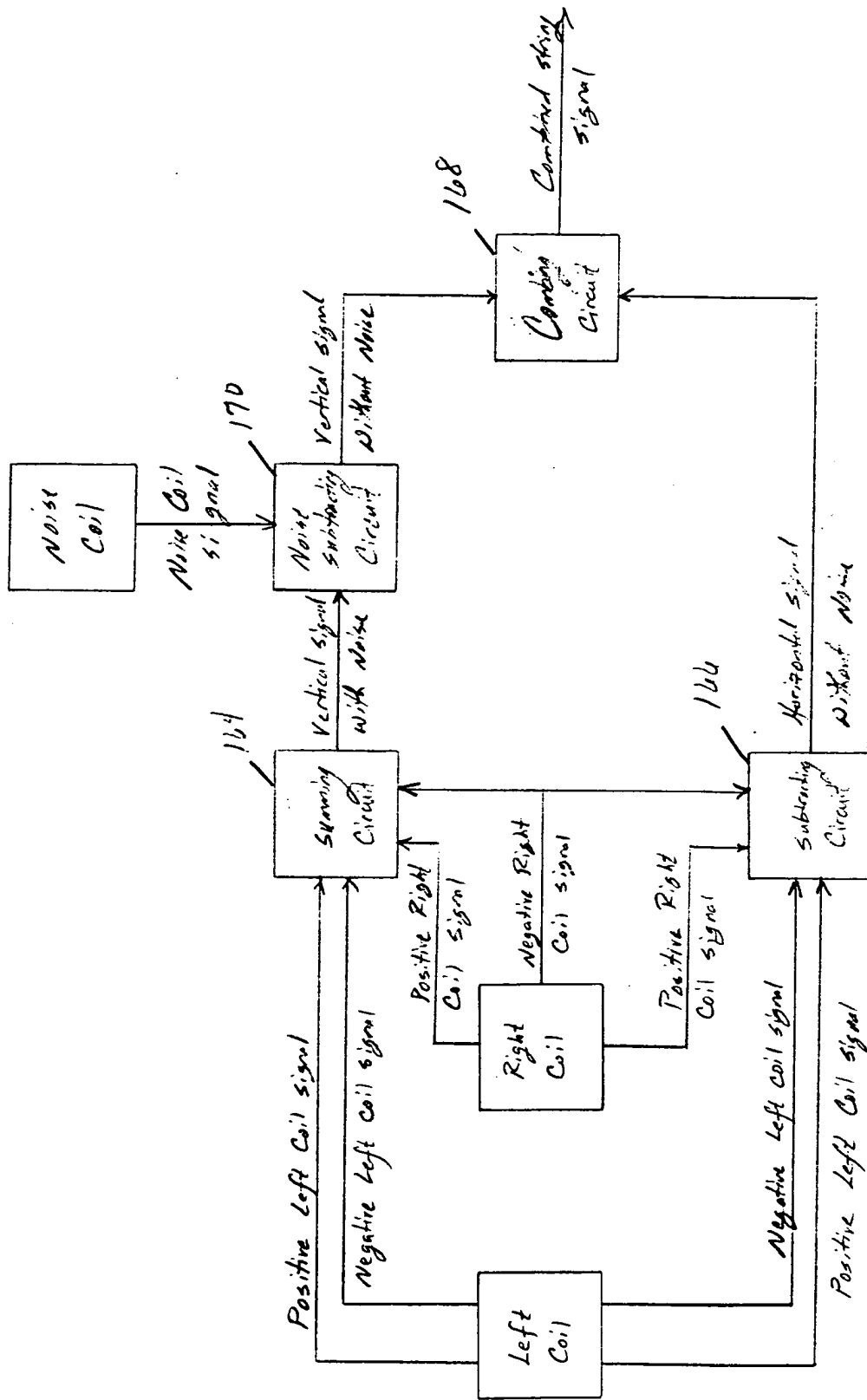


Fig. 10

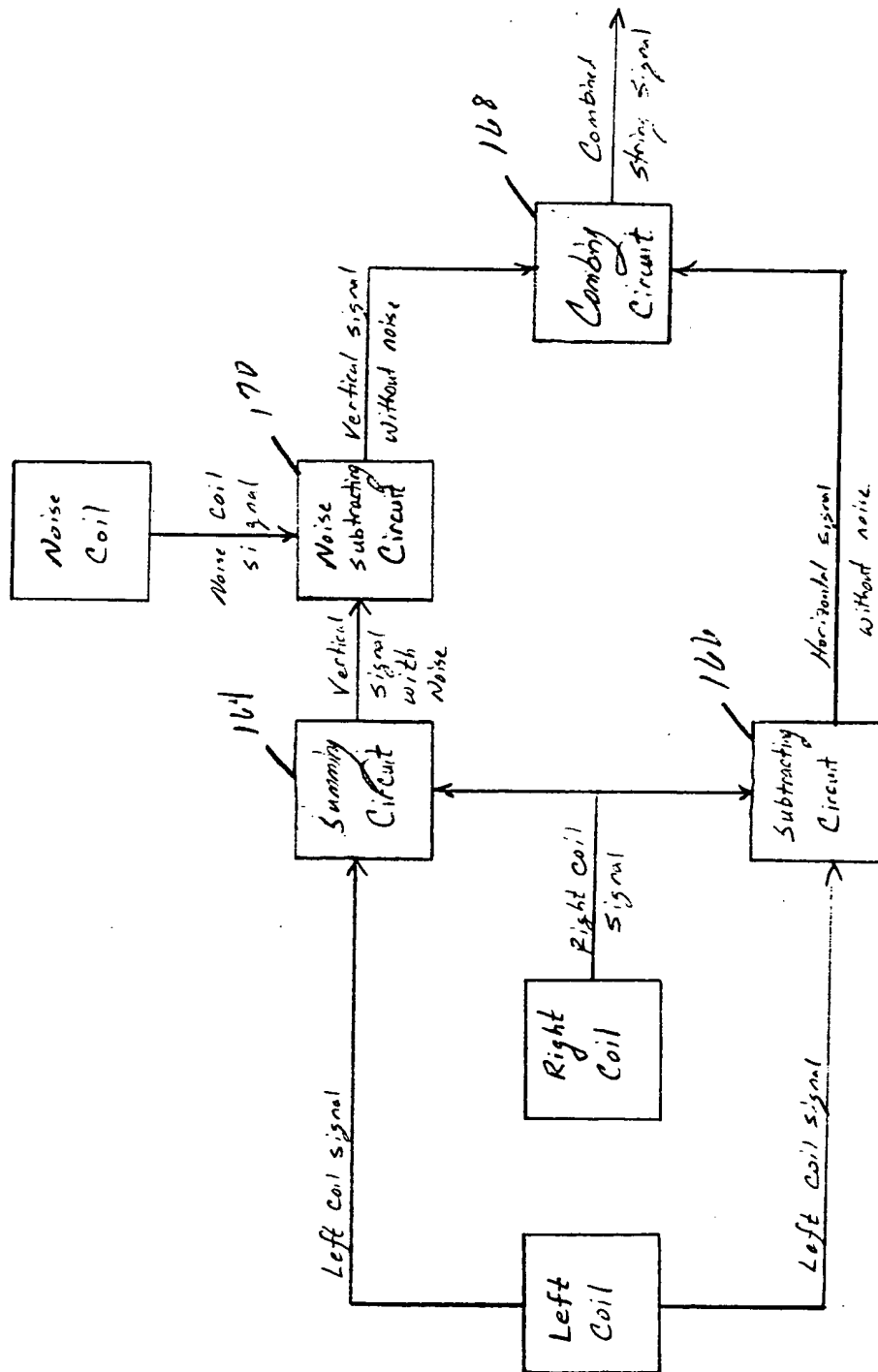


Fig. 11

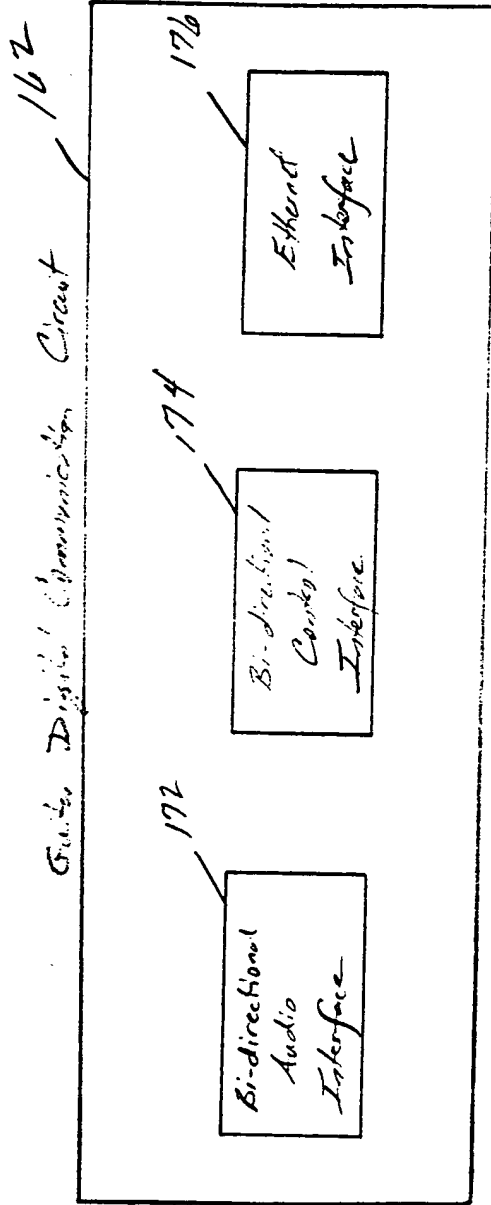


Fig. 12

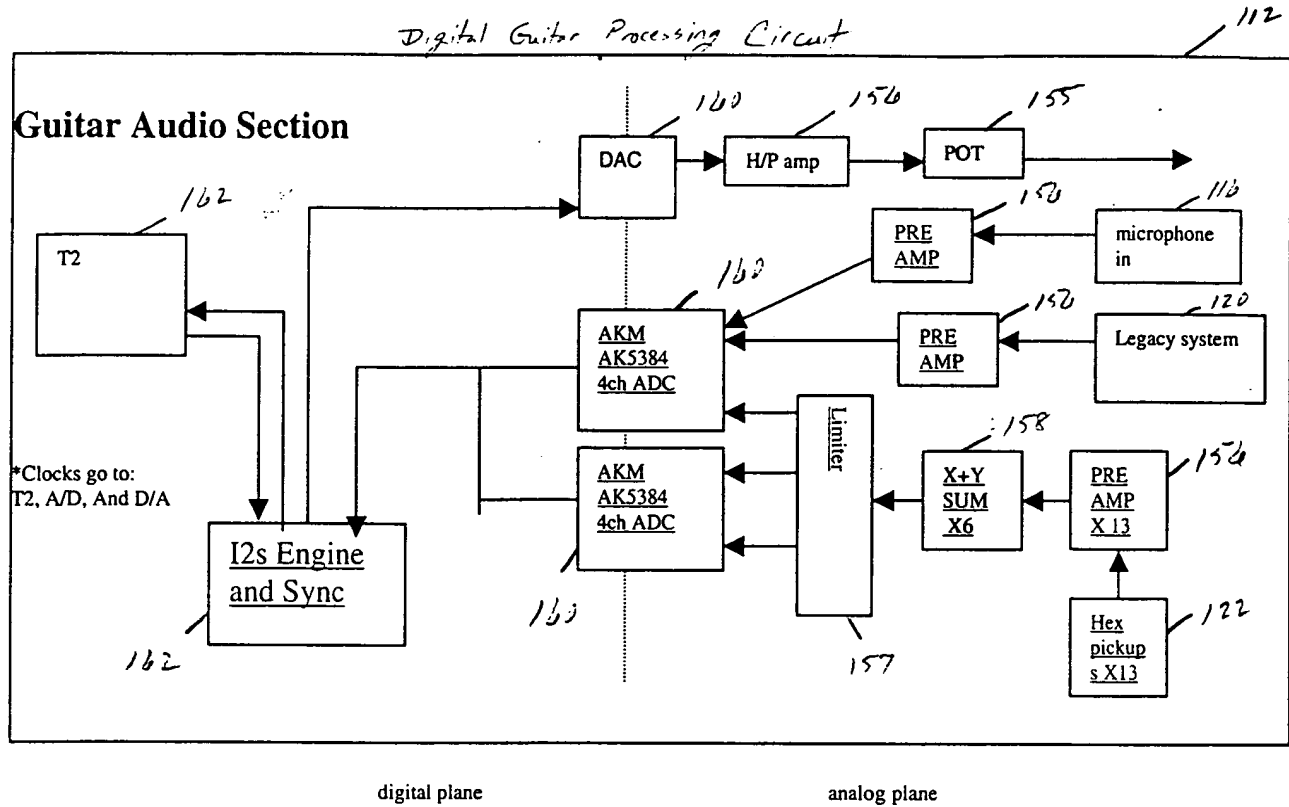


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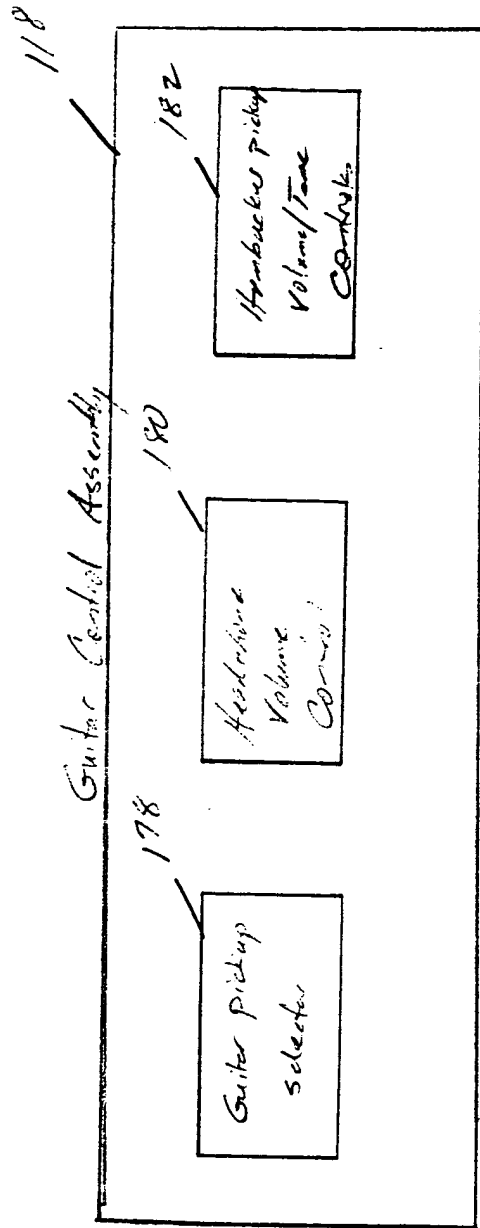


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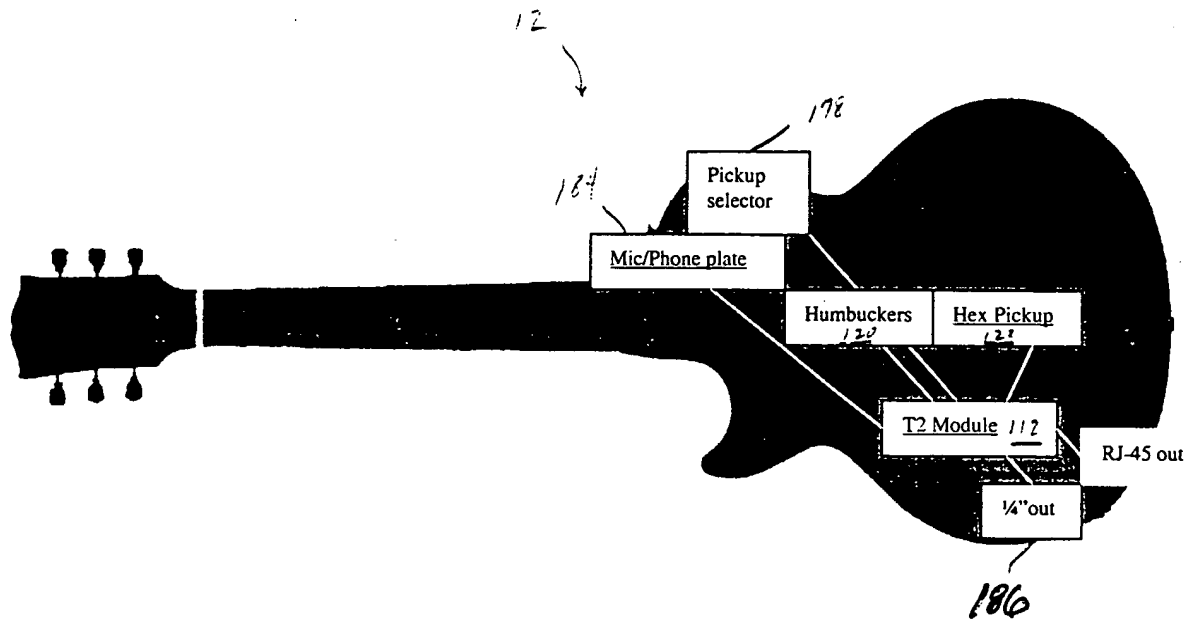
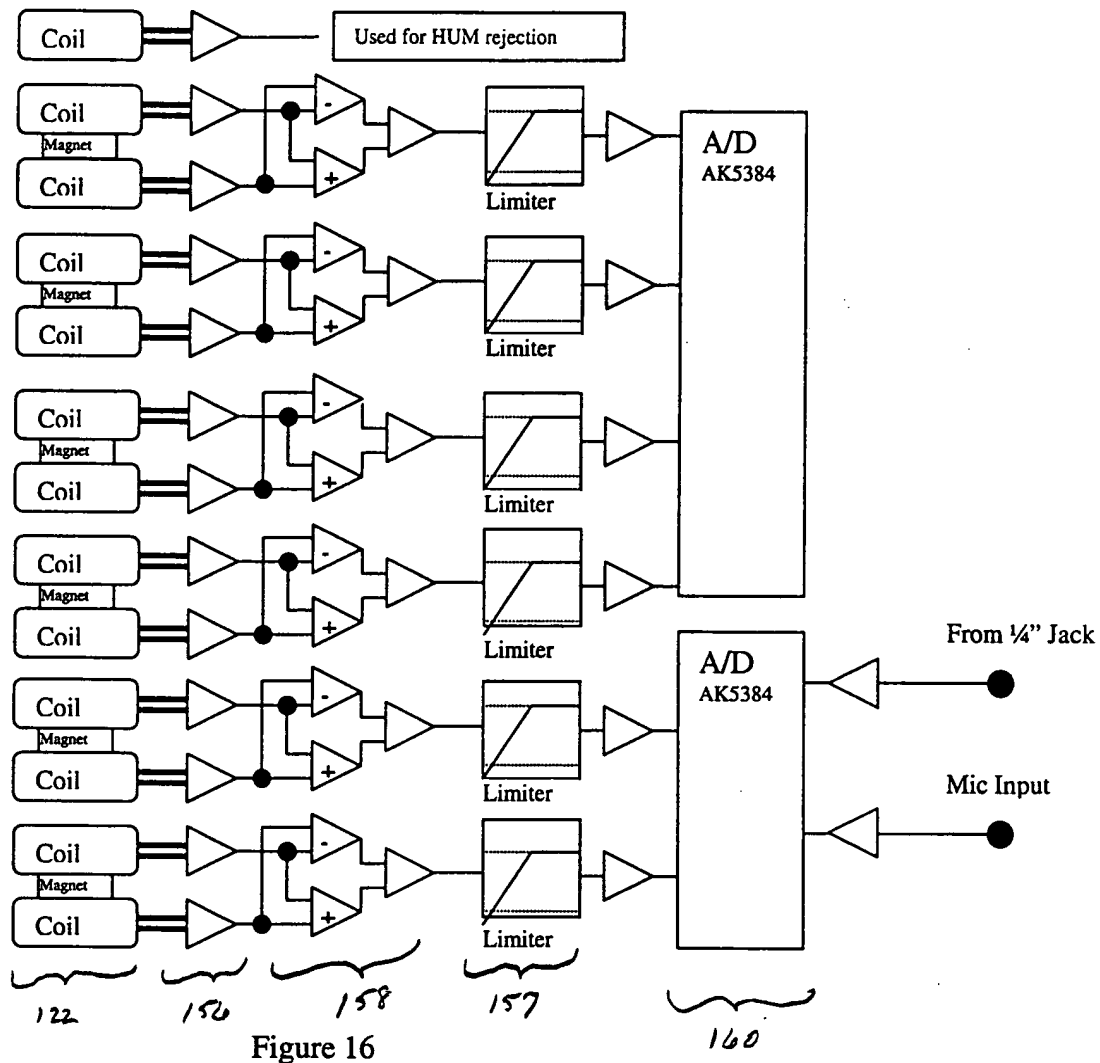


Figure 15



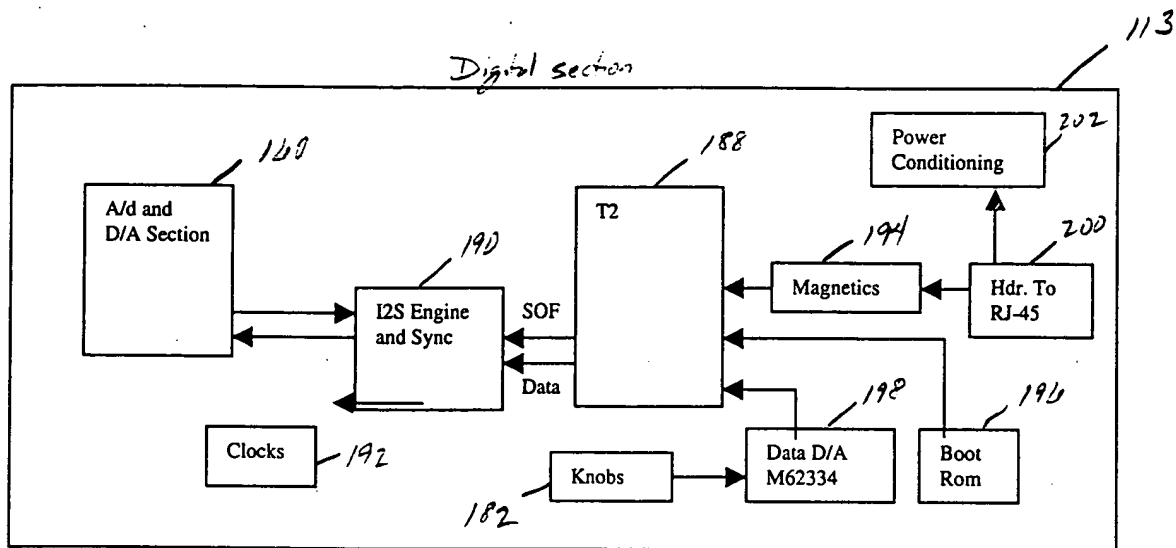


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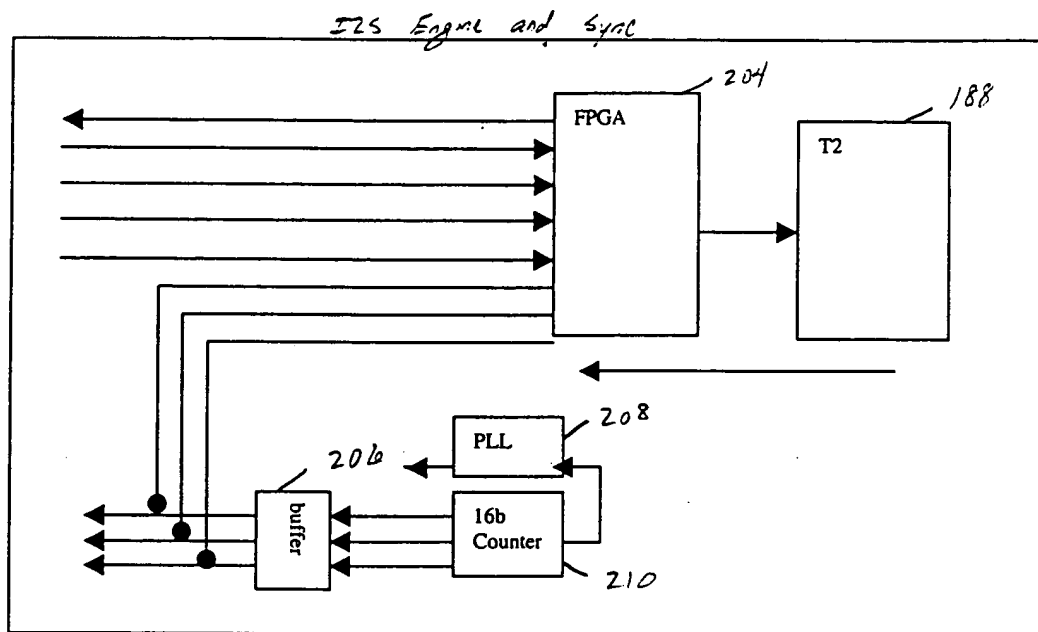


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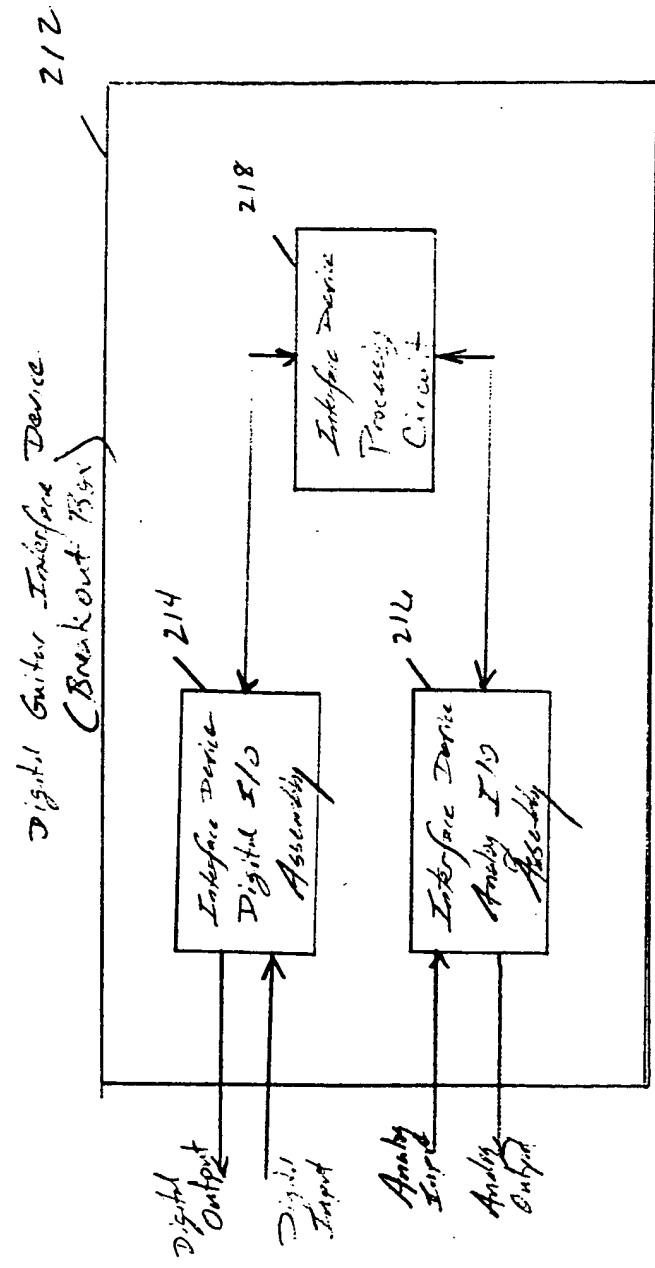


Fig. 19

Interface Device Processing Circuit

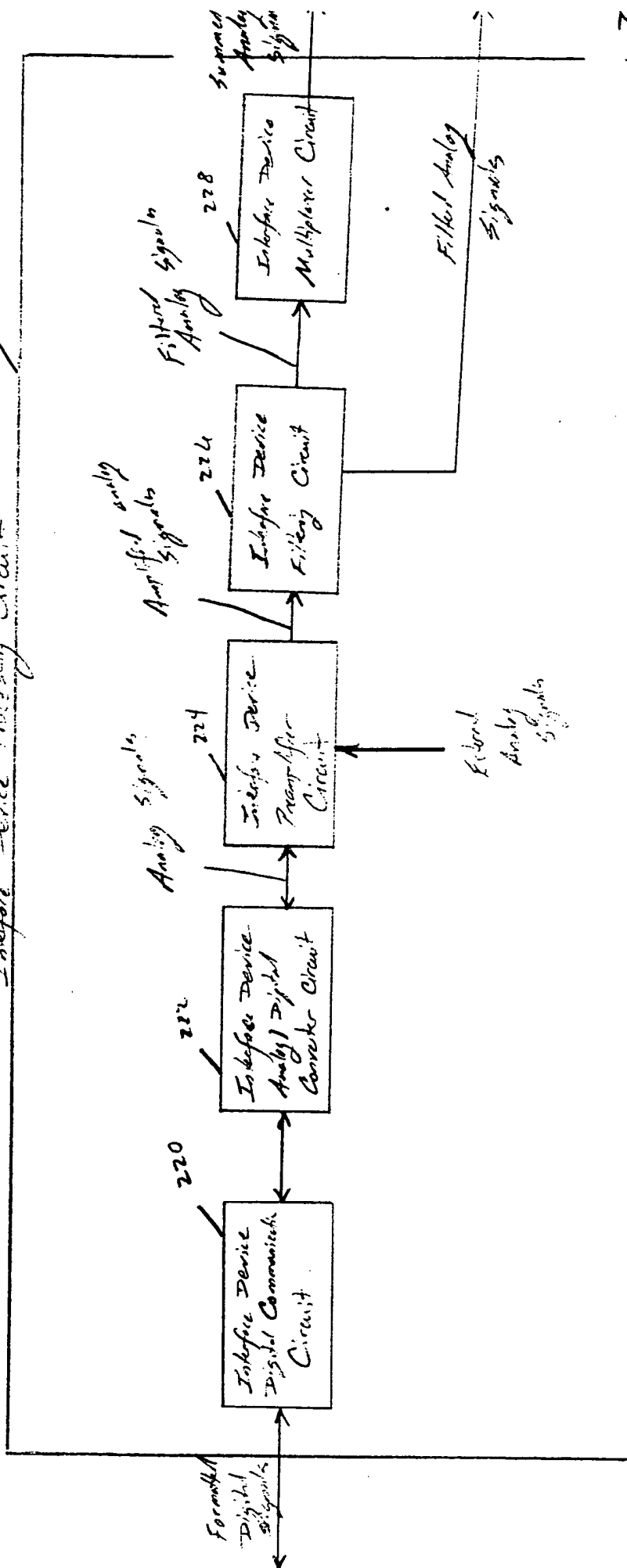
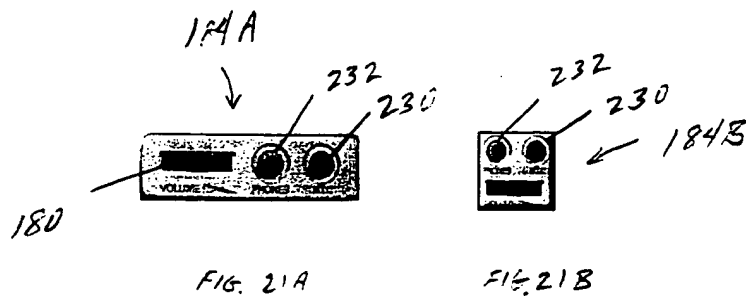


Fig. 20



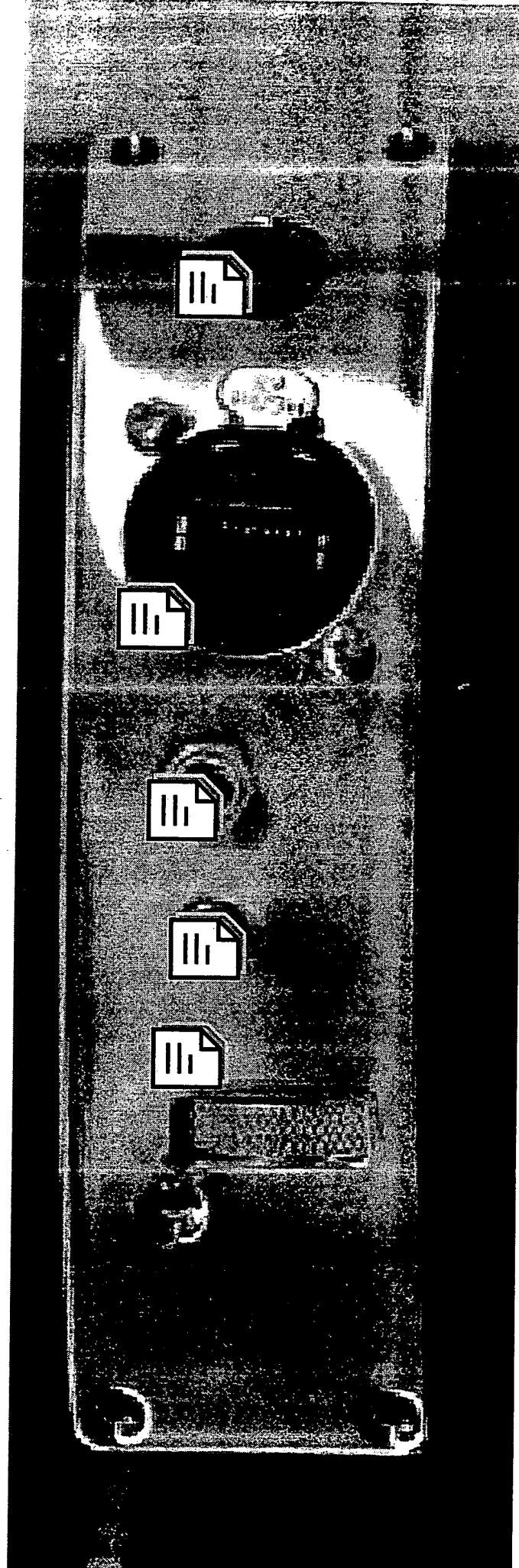


FIG. 21C

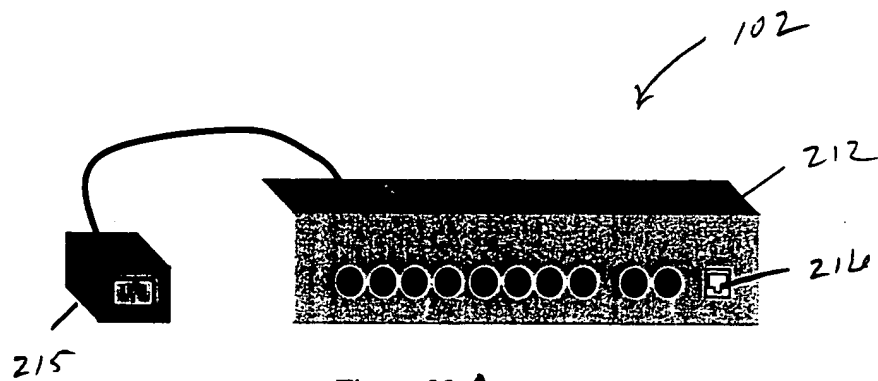


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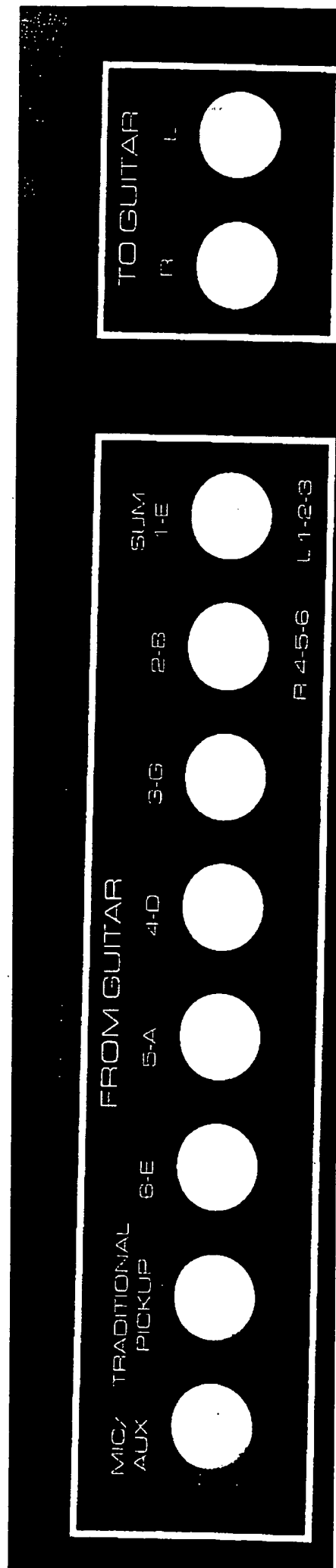


FIG. 22 B

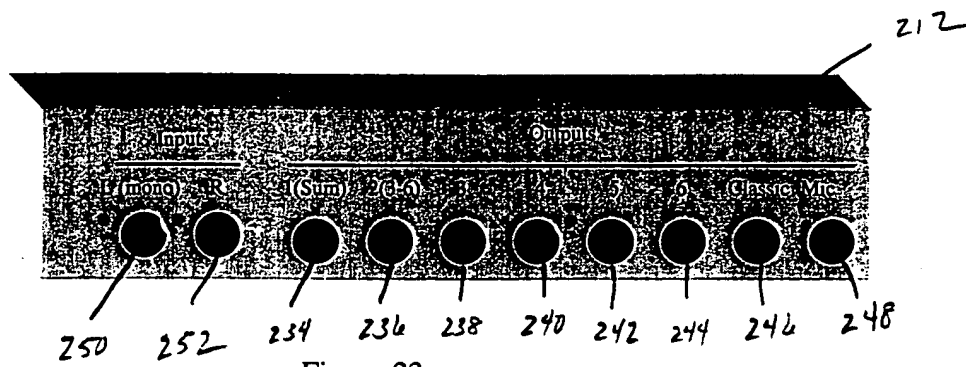


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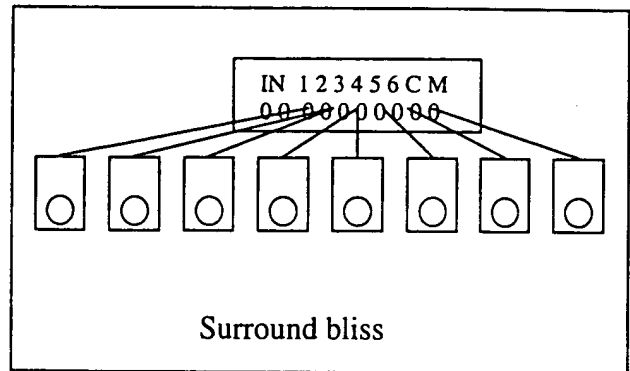
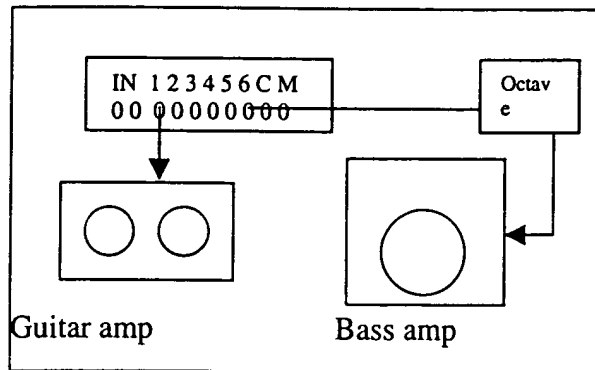
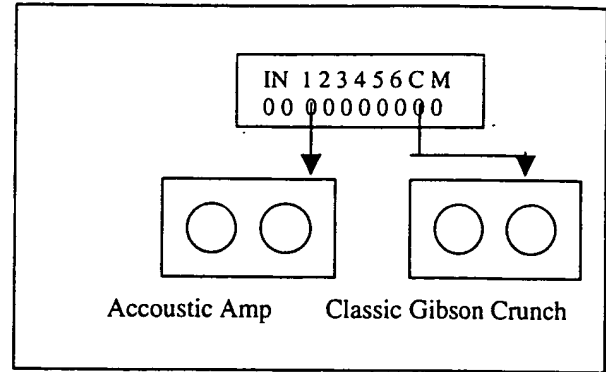
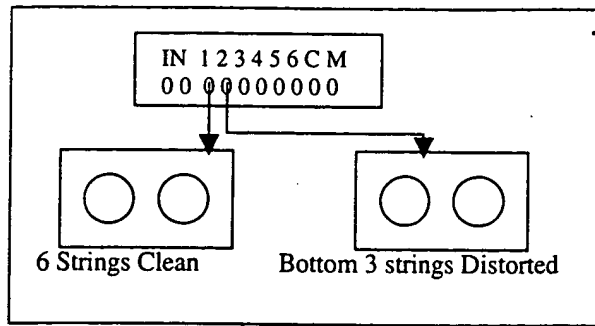


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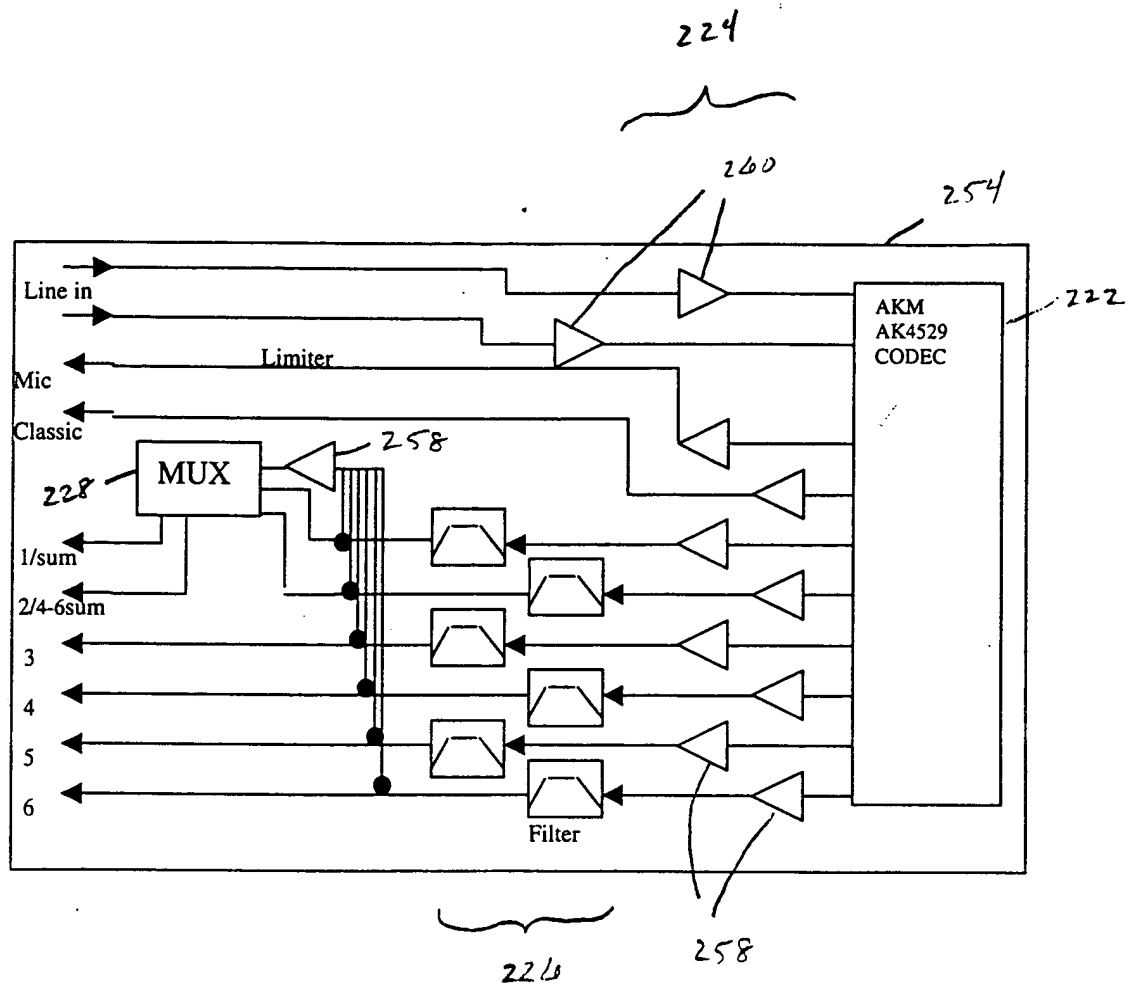


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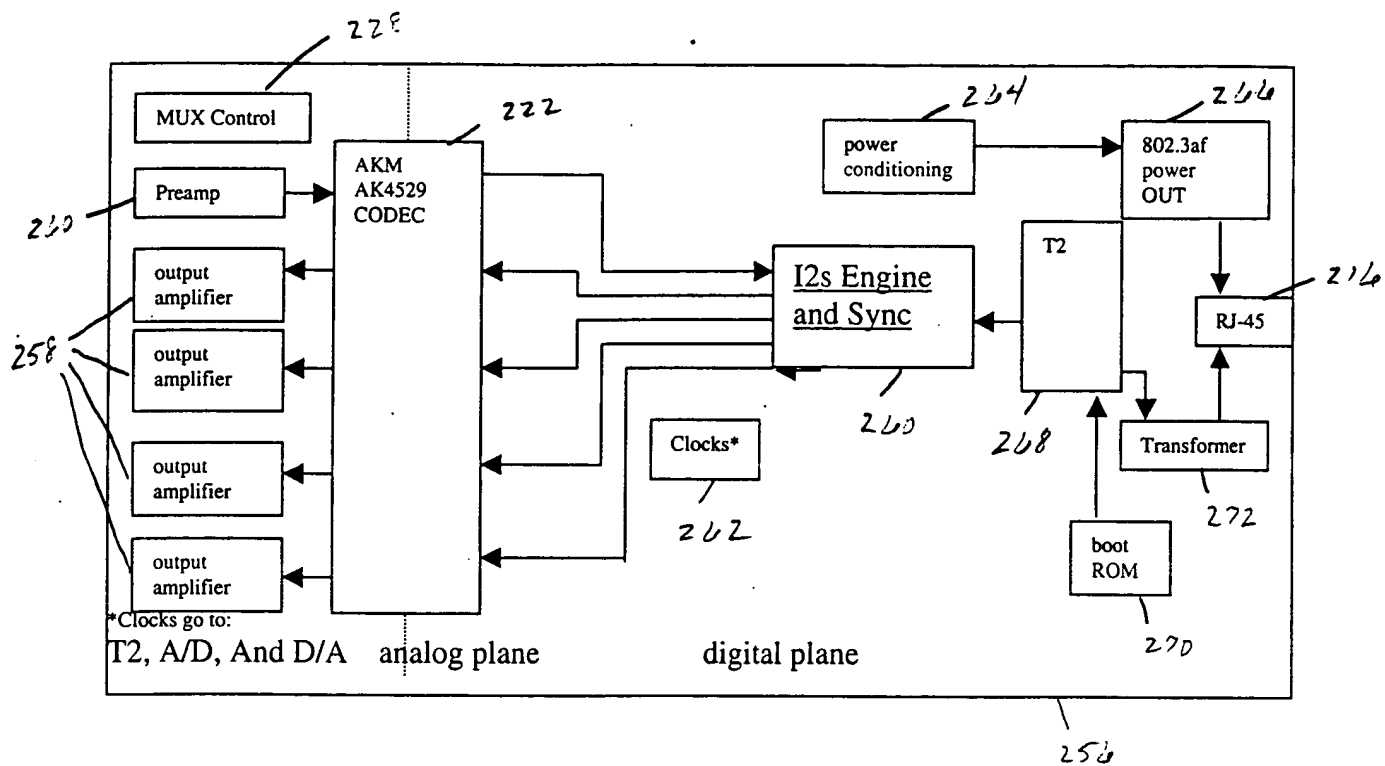


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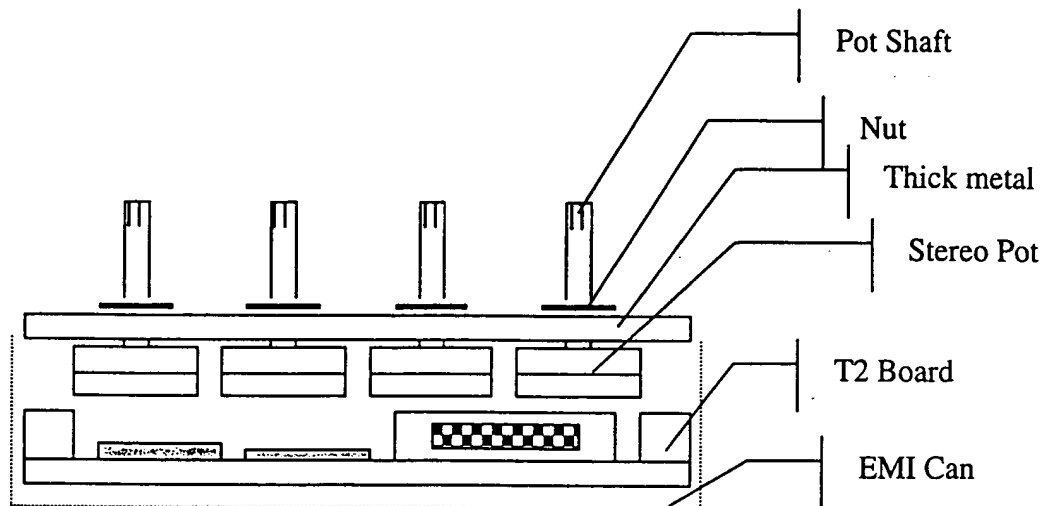


Figure 27

Passive Legacy system and Control Section

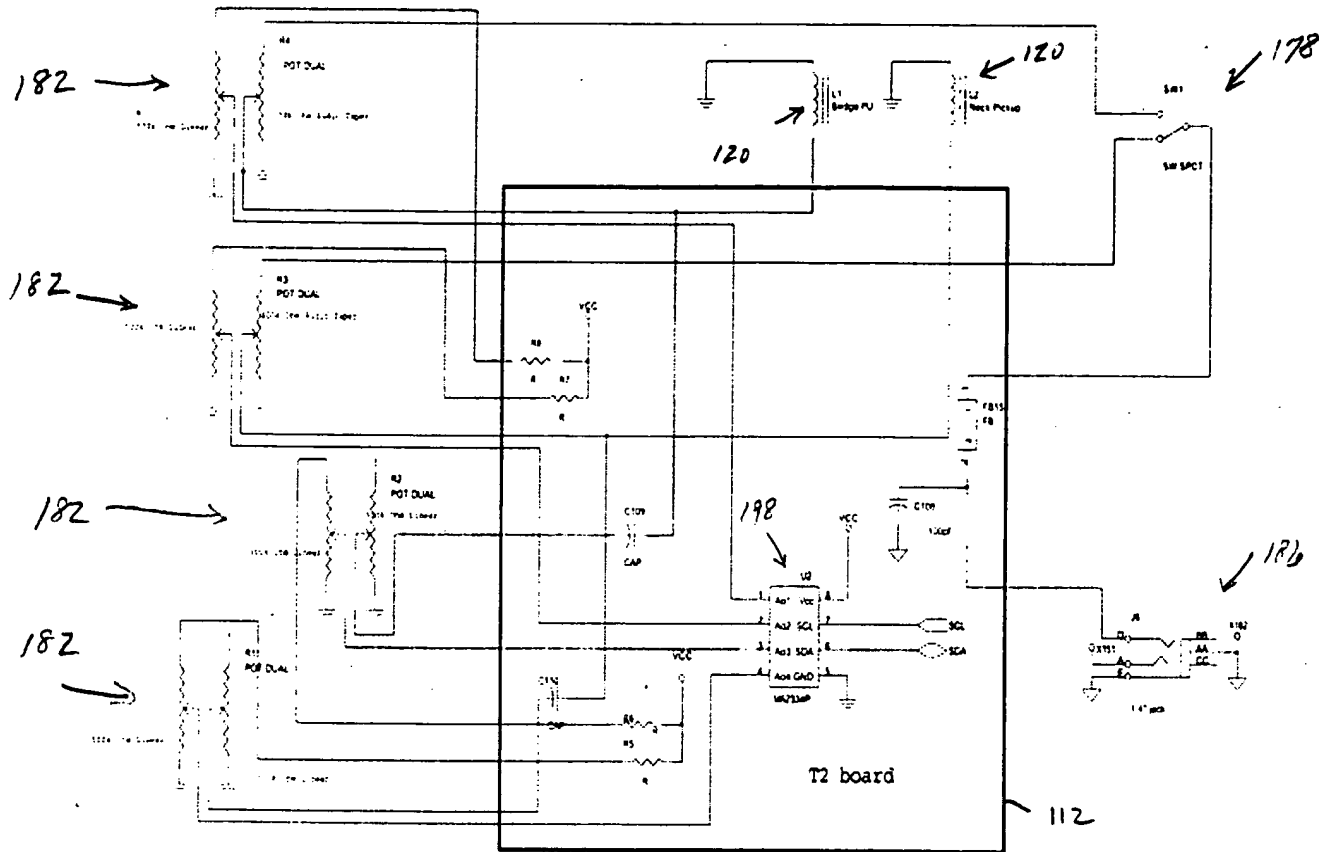
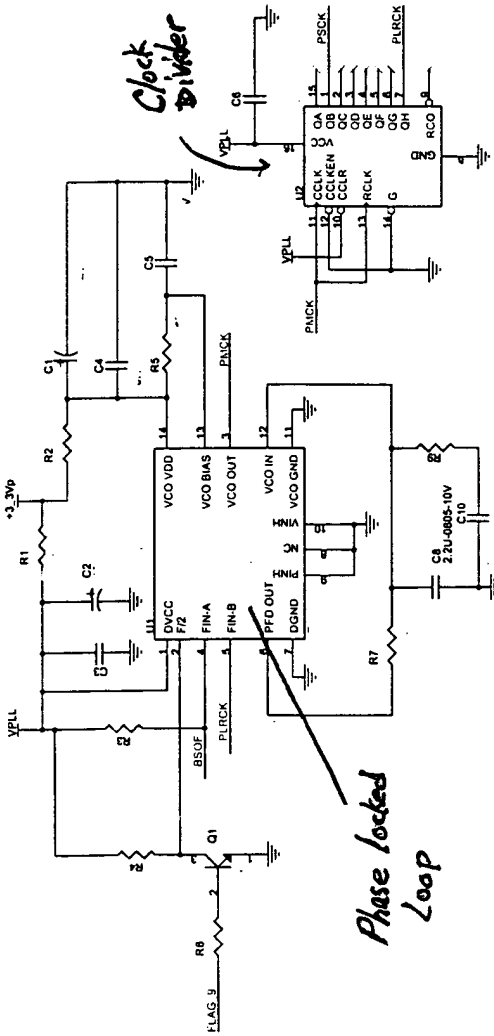


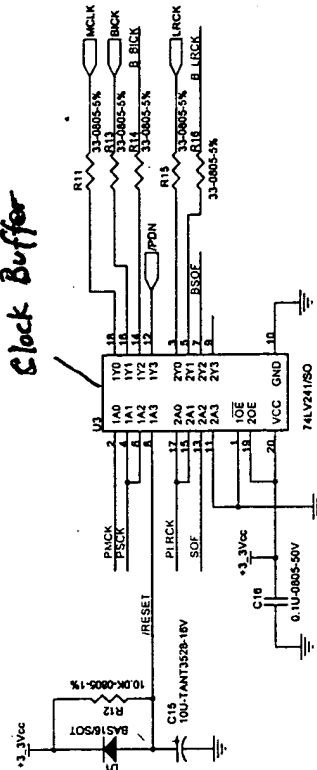
Figure 28

Clock Divider

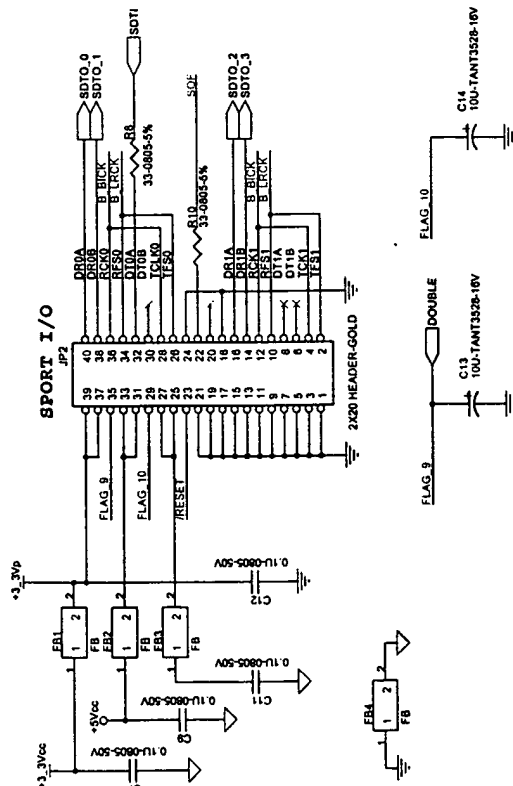
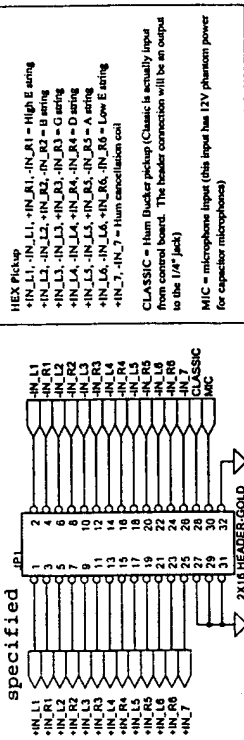


Phase locked
Loop

Clock Buffer

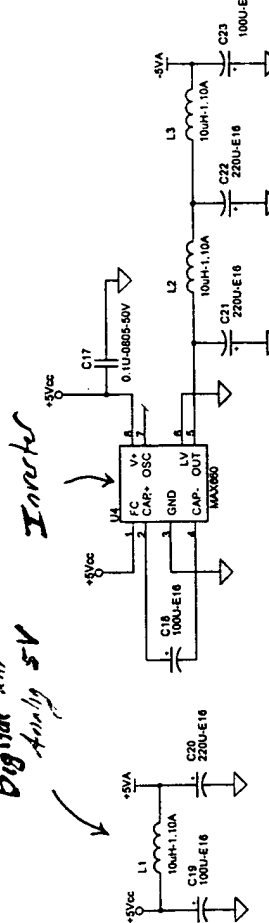


Connector to be



Digital and
Analog 5V

Invertebrates



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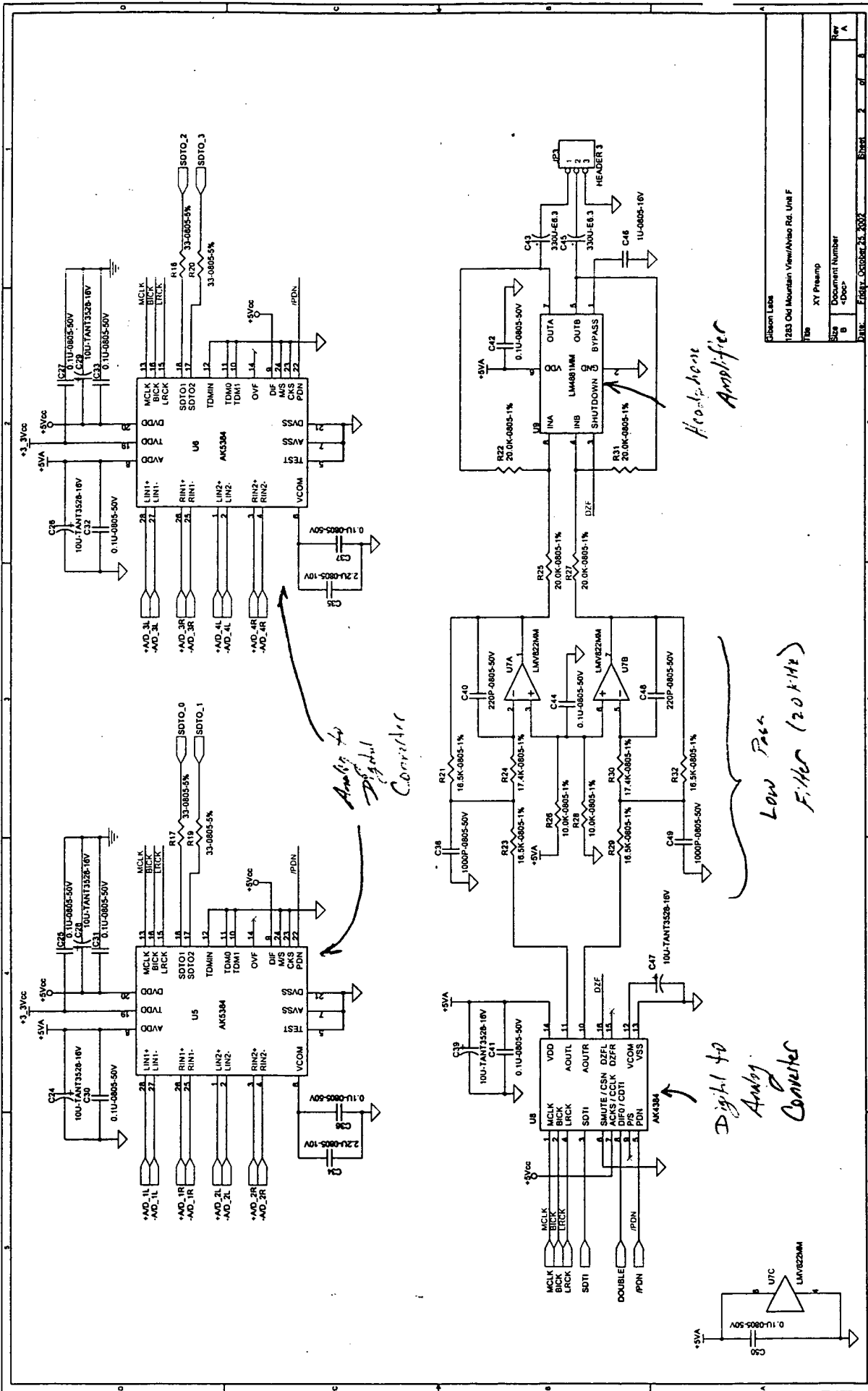
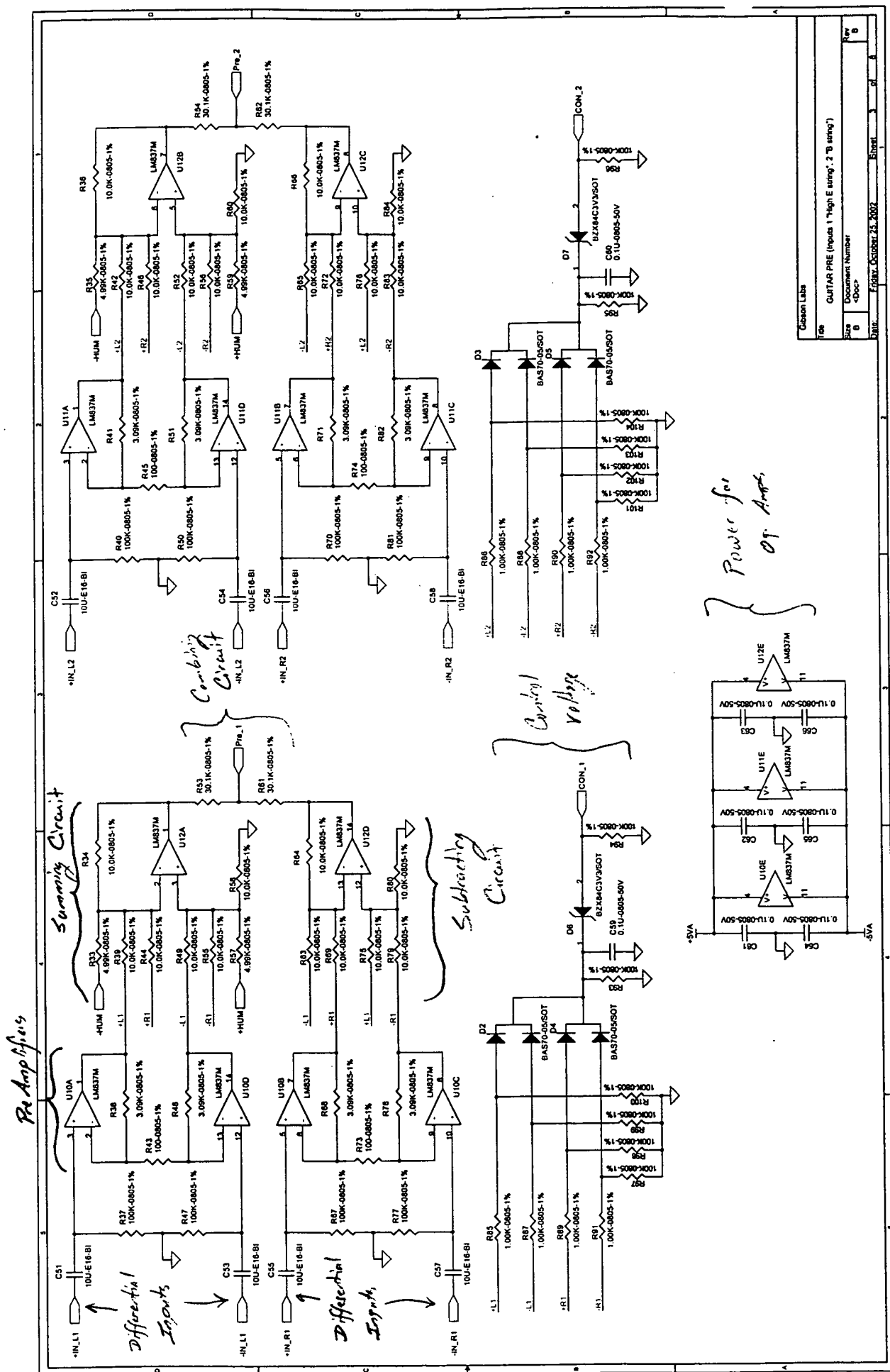


Fig. 30



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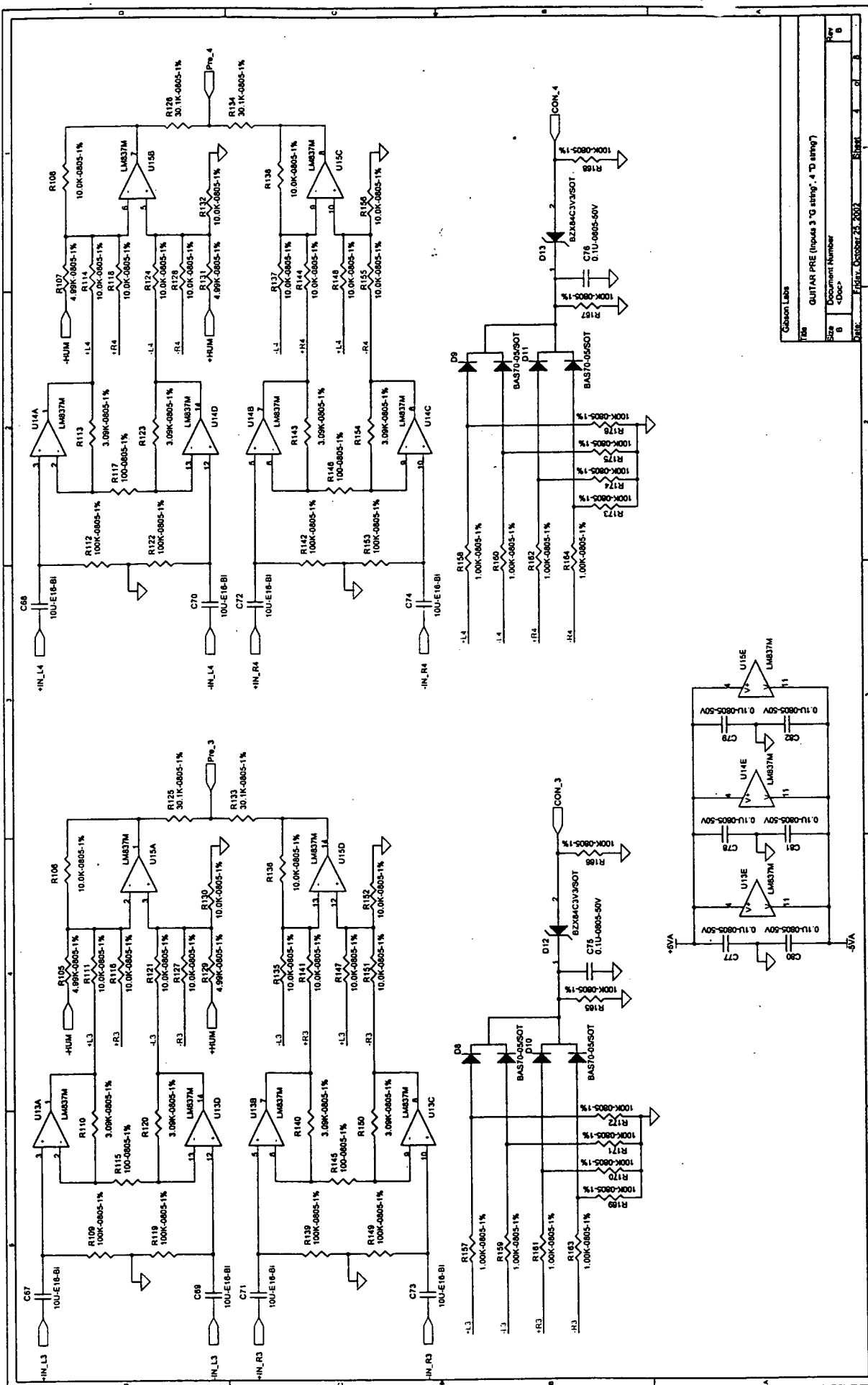
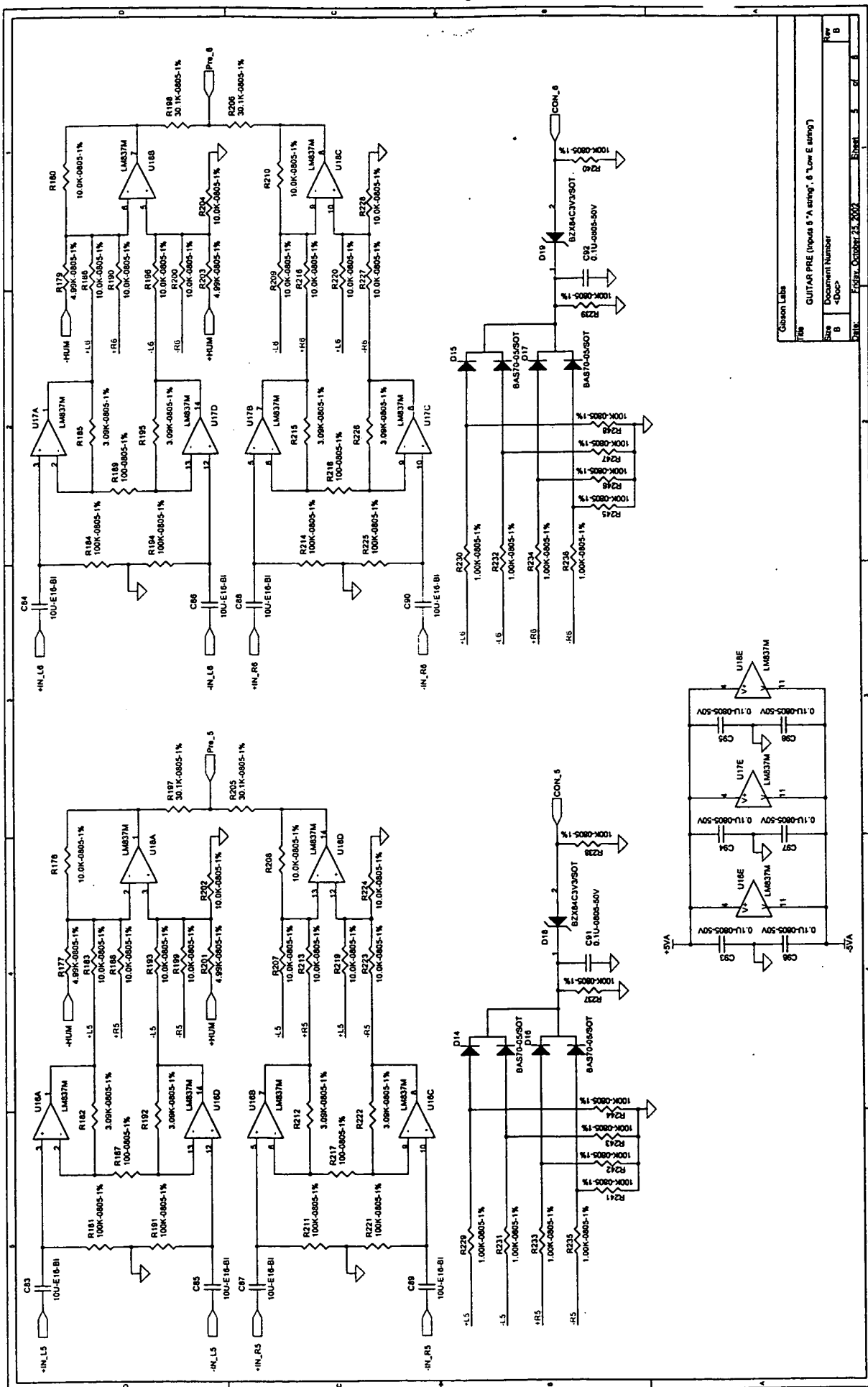


Fig. 32

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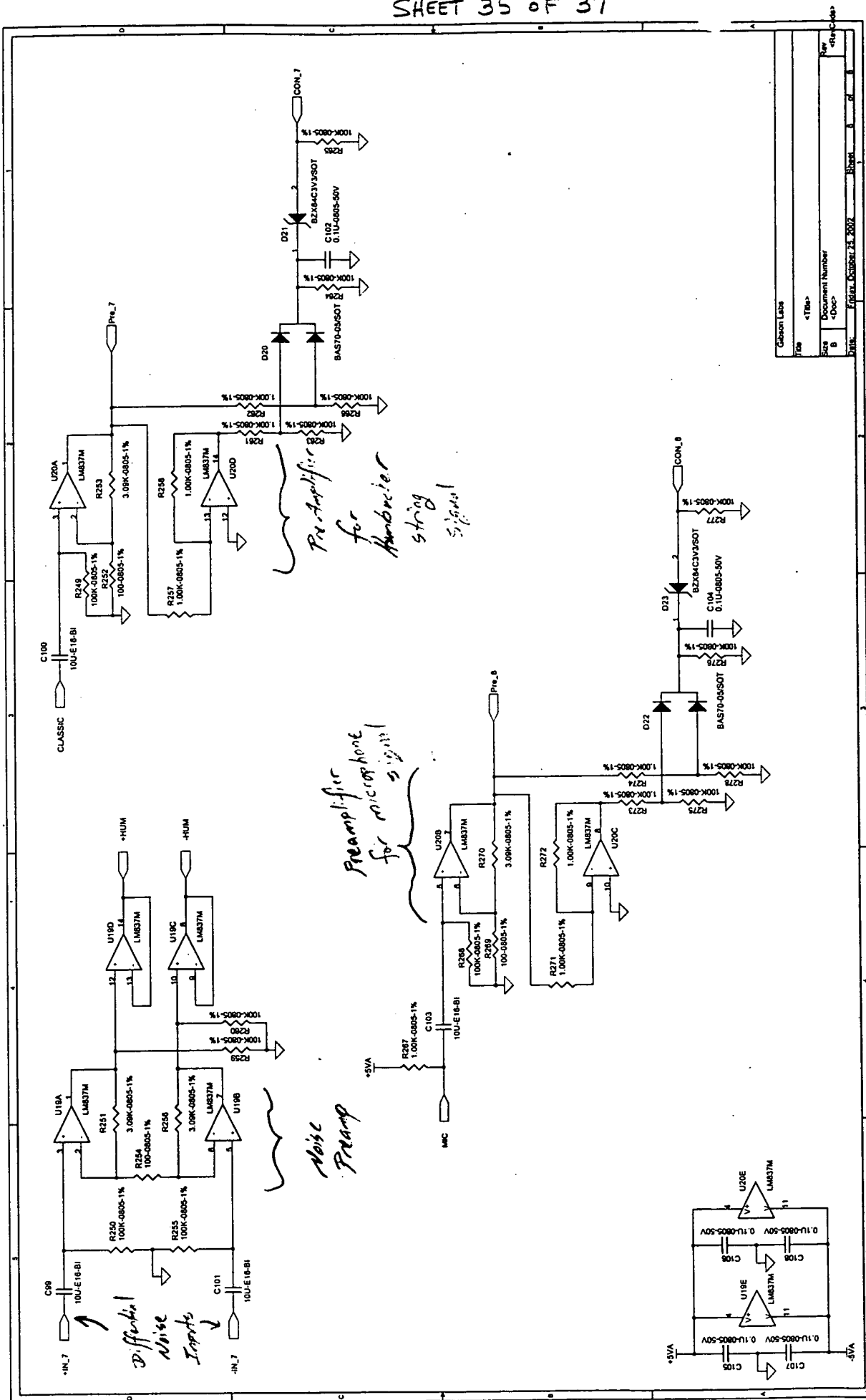


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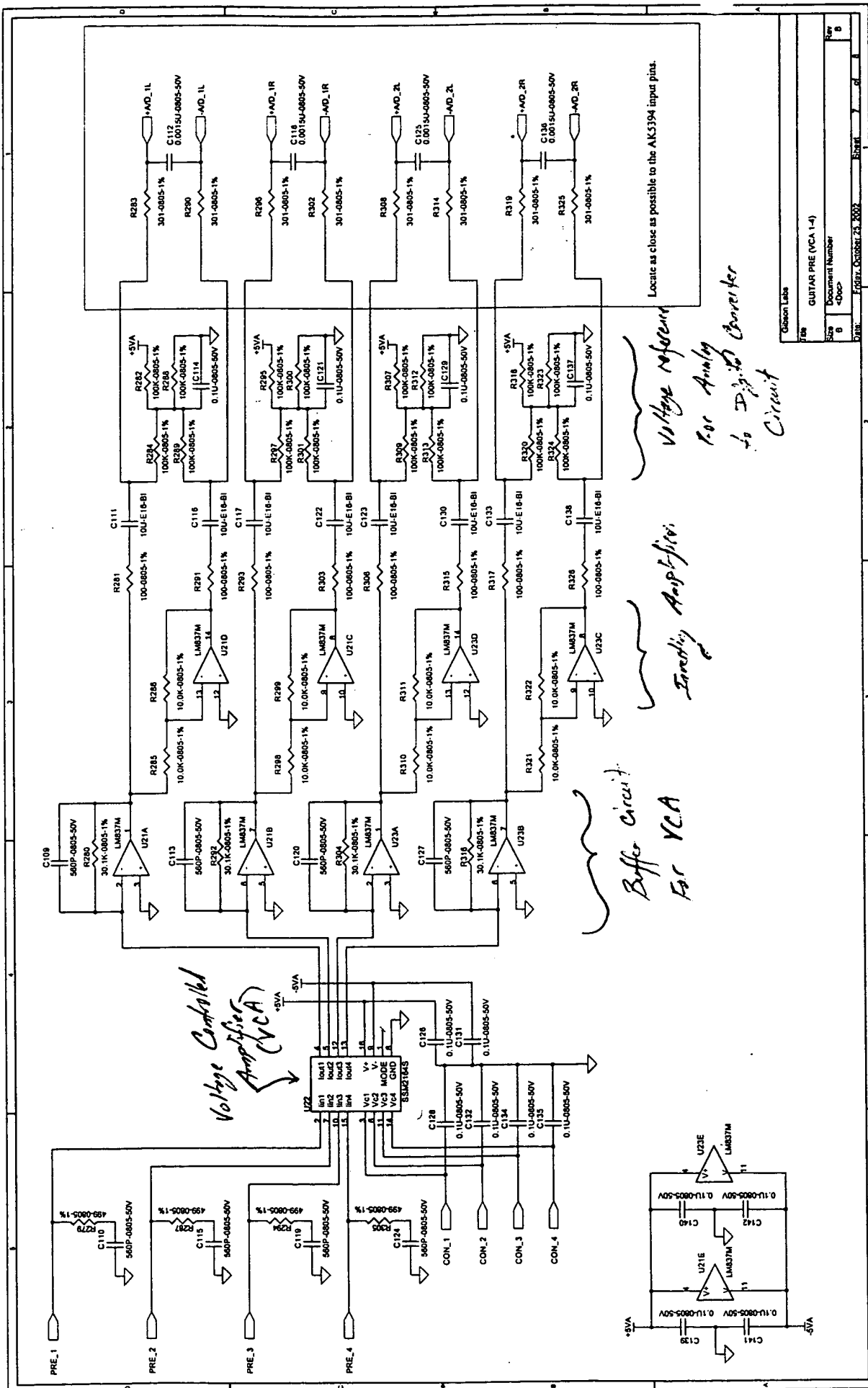


fig. 35

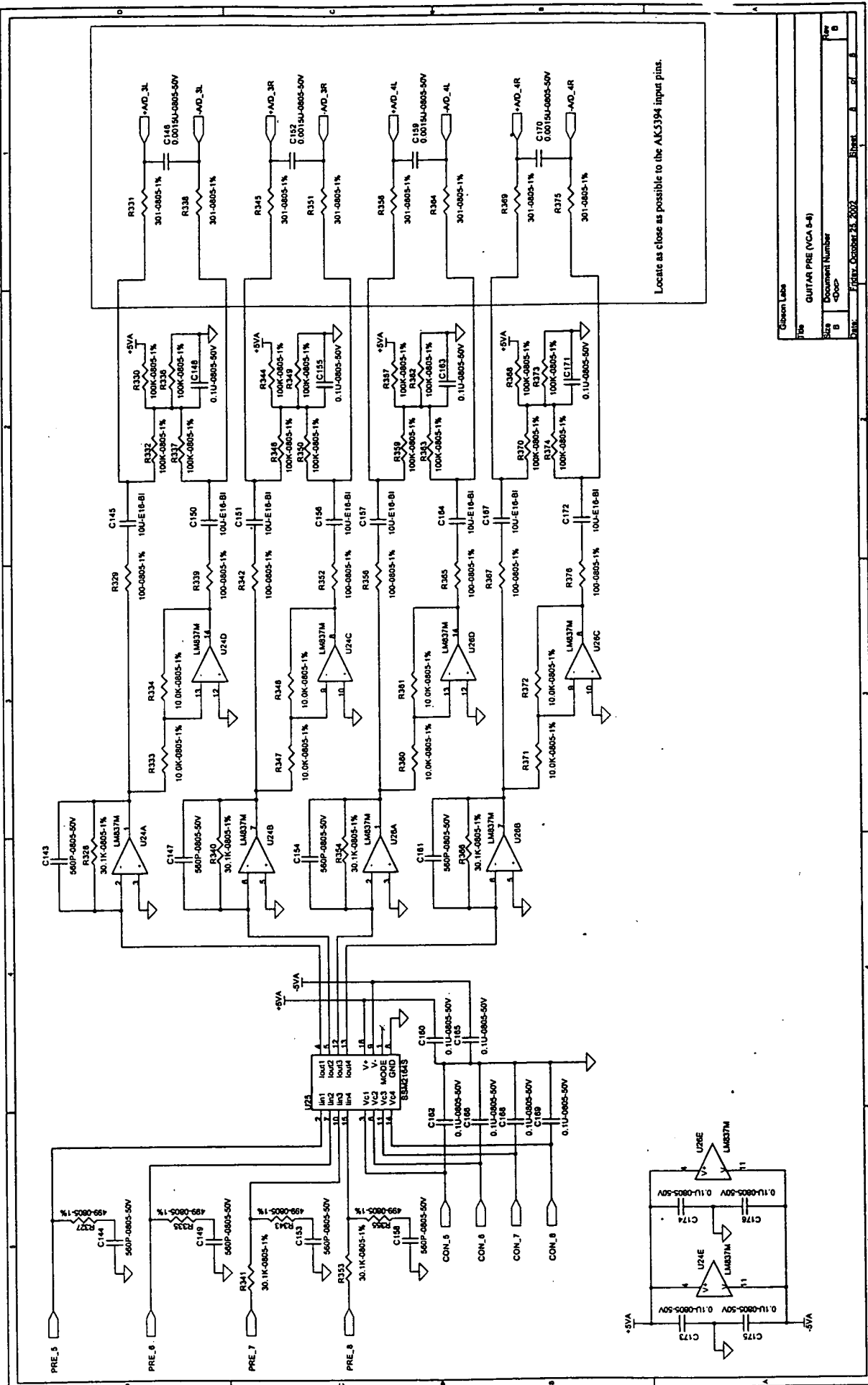


Fig 34

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